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*Published in:*  
I E E E Transactions on Power Electronics

*DOI (link to publication from Publisher):*  
[10.1109/TPEL.2020.3015540](https://doi.org/10.1109/TPEL.2020.3015540)

*Publication date:*  
2021

*Document Version*  
Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

*Citation for published version (APA):*  
Zheng, C., Dragicevic, T., Zhang, Z., Rodriguez, J., & Blaabjerg, F. (2021). Model Predictive Control of LC-Filtered Voltage Source Inverters With Optimal Switching Sequence. *I E E E Transactions on Power Electronics*, 36(3), 3422-3436. [9165198]. <https://doi.org/10.1109/TPEL.2020.3015540>

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# Model Predictive Control of $LC$ -Filtered Voltage Source Inverters With Optimal Switching Sequence

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**Abstract**—Voltage source inverters with output  $LC$  filter enable a sinusoidal output voltage with low harmonics, suitable for islanded ac microgrid or uninterruptible power supply applications. Conventional finite-set model predictive voltage control applies only a single switching vector per control period, leading to a variable switching frequency and significant output ripple. This paper resolves these issues by proposing an improved model predictive voltage control with optimal switching sequence (OSS-MPVC). First, an improved vector switching sequence is defined, aiming to reduce the output-voltage ripple with a constant switching frequency. Then, to tackle the difficulty in extending the OSS to high-order systems due to the coupling effect of the output filter, a generalized ‘one-step estimation’ solution is proposed, which directly associates the control-variable gradients with the vector switching sequence. To further enhance the output-voltage tracking accuracy, inter-sample dynamics are taken into account in the cost function. The control delay and dead-time compensation are also considered. Simulations and experimental results verify the feasibility of the proposed method.

**Index Terms**—Microgrid, inverters, model predictive control, fixed switching frequency, optimal switching sequence.

## I. INTRODUCTION

AC microgrid plays a significant role in the high penetration of distributed energy resources, which can be configured either in grid-connected or islanded mode. Voltage source inverters (VSIs) serve as crucial interfaces between ac microgrids and standalone loads or grids. When an ac microgrid operates in an islanded mode, VSIs are desired to continue to provide high-quality ac voltage for the loads, which are often controlled as grid-forming inverters to work as ideal ac voltage sources (e.g., uninterrupted power supplies) [1]. Compared to  $L$  or  $LCL$ -filtered VSIs,  $LC$ -filtered VSIs can attenuate the high-frequency harmonics while generating a sinusoidal output voltage, thus suitable for standalone applications [2]. In this context, it is vital to explore an effective control scheme that can achieve excellent output-voltage regulation performance with good steady-state accuracy (low ripple and total harmonic

distortion (THD)) and fast command-voltage dynamic tracking performance under various load conditions.

Conventionally, to achieve the desired output-voltage regulation, multi-loop linear controllers are usually deployed [3]. Although it is practically accepted, this control method has limited dynamic performance and time-consuming parameter-tuning processes due to the cascaded control loops. As a promising alternative, model predictive control owns exclusive advantages over linear methods, such as intuitive concept, fast dynamic response, and flexible tackling of multiple control objectives and constraints [4]–[8]. One important branch of model predictive control is finite-set model predictive control (FS-MPC). In general, the FS-MPC scheme makes the best of VSI’s discrete nature. It employs a discrete model to predict future system states and applies one optimal switching state obtained by minimizing a performance-dependent cost function. Nevertheless, several challenges hinder its application. Lack of modulation stage leads to significant output ripples, spread harmonic spectra (variable switching frequency), and unwanted triggering of resonances [4], [6], [7].

Several solutions have been presented to reduce the output ripple and/or achieve a fixed switching frequency of FS-MPC schemes. Regarding output ripple reduction, one solution is to increase the prediction horizon, in which the computational burden is significantly raised [9]. There exist solutions for computationally efficient enumeration, but they require a high level of expertise in control theory to understand and implement [10]. Another solution is to modify the cost function. In [11], an integral-error tracking term is added into the cost function, which reduces the steady-state tracking error. In [12], a digital filter is embedded in the cost function to shape the output harmonic spectrum. Similarly, a selective harmonic elimination technique is incorporated into FS-MPC schemes in [13], effectively decreasing the lower-order harmonics. Nonetheless, all of the aforementioned strategies still inherit the problems of the variable switching frequency in conventional FS-MPC schemes, which may cause a spread harmonic spectrum and complex design of output filter.

On the other hand, various fixed-switching-frequency MPC schemes have been proposed [14], [15]. In [14], a deadbeat MPC scheme is proposed. This approach is essentially a continuous-set MPC, and the fixed switching frequency is directly obtained by a modulator. In [15], a switched MPC scheme is proposed, which is implemented by employing the FS-MPC to quickly track the reference during transients while switching to a modulated MPC during steady state. However, the switching threshold is not easy to determine, which may

Manuscript received Month xx, 2020; revised Month xx, 2020; accepted Month x, 2020. (Corresponding author: Changming Zheng.)

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cause false triggering. Recently, instead of performing a single voltage vector as conventional FS-MPC schemes, multi-vector MPC schemes are proposed to produce a constant switching frequency [16]–[20]. In [16], a discrete space-vector-modulation based FS-MPC is proposed. However, a significant computational burden is induced due to the numerous virtual vectors, making it challenging to implement in real-time systems. In [17], a two-vector MPC scheme is proposed for torque control of inductive motors. Two voltage vectors with optimal duty cycles are performed per control period, achieving improved steady-state accuracy with a quasi-constant switching frequency. Nevertheless, the control degree of freedom is still limited, and the optimal steady-state performance cannot be guaranteed. In [18], a fixed-switching-frequency multi-vector MPC scheme is proposed for  $L$ -filtered grid converters. A vector switching sequence is performed per control period, enhancing the steady-state performance. Moreover, an optimal switching sequence concept is introduced to multi-vector MPC schemes to further reduce the output ripples [19]–[21]. Essentially, the optimal switching sequence provides an optimal way to select the vector switching sequence to be applied. As a result, the steady-state performance is optimal with a constant switching frequency. Nonetheless, all existing optimal-switching-sequence based MPC strategies are designed solely for first-order  $L$ -filtered VSIs [19]–[21]. To the best of our knowledge, no reference has reported this control strategy for high-order systems, such as  $LC$  or  $LCL$ -filtered VSIs. One of the key reasons is that the cross-coupling effect of  $LC$  filter is complex to explicitly embed in the design procedure of optimal switching sequence. To be specific, for  $L$ -filtered VSIs, the state variable (inductor current) is directly controlled by inverter voltage. Hence, a vector switching sequence can be directly performed to calculate the inductor-current gradient. In contrast, for  $LC$ -filtered VSIs, due to the cross-coupling effect between the inductor current and capacitor voltage, the capacitor-voltage gradient cannot be simply obtained by the inverter voltage vector [22]. Consequently, direct implementation of the optimal switching sequence for output voltage control of  $LC$ -filtered VSIs becomes very challenging. This challenge also exists in higher-order systems, including current/power control of  $LCL$ -filtered grid-tied VSIs.

To tackle the issues above, this paper proposes an improved model predictive voltage control with optimal switching sequence (OSS-MPVC) for  $LC$ -filtered VSIs. The contributions are summarized as follows:

1) The OSS-based MPC algorithm is extended to output-voltage control of a second-order  $LC$ -filtered VSI, enabling the system to operate with improved output-voltage performance and a constant switching frequency.

2) A ‘one-step estimation’ strategy is proposed to solve the voltage-gradient calculation challenge caused by the state-coupling of  $LC$  filter. It provides a generalized way to calculate the control-variable gradient, making it possible to extend the application scope of OSS to the higher-order systems, such as  $LCL$ -filtered VSIs.

3) An improved vector switching sequence is proposed, increasing the voltage control degrees of freedom, and reducing output ripple and computational burden compared to prior

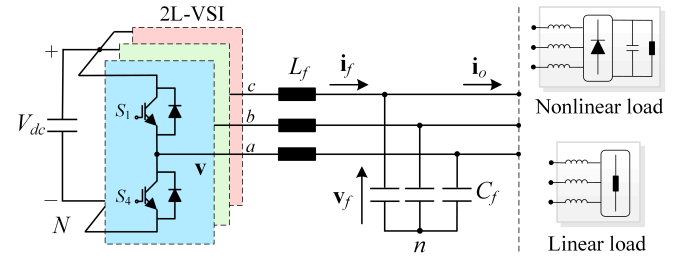


Fig. 1. Typical topology of an  $LC$ -filtered standalone VSI.

TABLE I  
SWITCHING STATES AND VOLTAGE VECTORS OF A VSI

Index $x$	Switching state $S_x$			Voltage vector $\mathbf{v}_x$	
	$S_{a,x}$	$S_{b,x}$	$S_{c,x}$	$v_{\alpha,x}$	$v_{\beta,x}$
0	{0	0	0}	0	0
1	{1	0	0}	$2V_{dc}/3$	0
2	{1	1	0}	$V_{dc}/3$	$\sqrt{3}V_{dc}/3$
3	{0	1	0}	$-V_{dc}/3$	$\sqrt{3}V_{dc}/3$
4	{0	1	1}	$-2V_{dc}/3$	0
5	{0	0	1}	$-V_{dc}/3$	$-\sqrt{3}V_{dc}/3$
6	{1	0	1}	$V_{dc}/3$	$-\sqrt{3}V_{dc}/3$
7	{1	1	1}	0	0

OSS-MPC schemes.

4) The inter-sample dynamics of the output voltage are explicitly considered in the cost function, further enhancing the steady-state voltage tracking accuracy.

The rest of this paper is organized below. The system description is given in Section II. Section III describes the conventional FS-MPC scheme and its limitations. Section IV elaborates the principle of the proposed OSS-MPVC. Section V gives the simulation and experimental results, and the whole work is concluded in Section VI.

## II. SYSTEM DESCRIPTION

### A. Working Principle and Control Objectives

The typical topology of an  $LC$ -filtered VSI is shown in Fig. 1. First, for a typical three-phase VSI without an output  $LC$  filter, its output phase voltage can be derived as [8]

$$\begin{cases} v_{an} = \frac{V_{dc}}{3} (2S_a - S_b - S_c) \\ v_{bn} = \frac{V_{dc}}{3} (2S_b - S_a - S_c) \\ v_{cn} = \frac{V_{dc}}{3} (2S_c - S_a - S_b) \end{cases} \quad (1)$$

where  $V_{dc}$  is the dc-link voltage, and the three-phase switching states are

$$S_a = \begin{cases} 1, & S_1 \text{ on}, S_4 \text{ off} \\ 0, & S_1 \text{ off}, S_4 \text{ on} \end{cases} \quad (2)$$

$$S_b = \begin{cases} 1, & S_2 \text{ on}, S_5 \text{ off} \\ 0, & S_2 \text{ off}, S_5 \text{ on} \end{cases} \quad (3)$$

$$S_c = \begin{cases} 1, & S_3 \text{ on}, S_6 \text{ off} \\ 0, & S_3 \text{ off}, S_6 \text{ on} \end{cases} \quad (4)$$

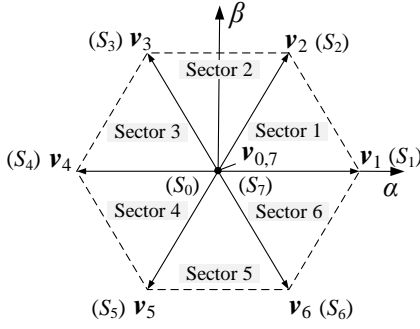


Fig. 2. Voltage vectors and sector division of a VSI.

where the upper-leg switching state  $S = \{S_a, S_b, S_c\}$  of are modeled as on “1” and off “0”. For a VSI, there are eight possible switching states and eight inverter voltage vectors  $\mathbf{v}_x = v_{\alpha,x} + jv_{\beta,x}$  with  $x \in \{0, 1, \dots, 7\}$  ( $\mathbf{v}_0 = \mathbf{v}_7 = 0$ ), which are expressed in complex  $\alpha\beta$  frame as in Table I and Fig. 2.

It can be seen from (1) that the direct output voltage of a VSI is a pulse waveform, which contains a large amount of switching harmonics. To generate a sinusoidal output voltage regulation for linear or nonlinear loads in islanded ac microgrid or uninterruptible power supply applications, a low-pass  $LC$  filter is normally connected to a VSI. Then, by selecting an appropriate cut-off frequency of the  $LC$  filter, the high-frequency harmonics can be significantly attenuated and a sinusoidal voltage can be obtained from the filter capacitance. Hence, the critical control objectives of this paper are to achieve excellent output voltage steady-state tracking performance (with low ripple and THD) and fast dynamic tracking response under load variations, especially under load step change and nonlinear load conditions.

### B. Dynamic Model

To facilitate the representation of a balanced three-phase VSI system, an amplitude-invariant Clarke transformation is employed to convert the capacitor voltage, inductor current, inverter voltage and load current from the three-phase  $abc$  frame to stationary  $\alpha\beta$  frame as  $\mathbf{v}_f$ ,  $\mathbf{i}_f$ ,  $\mathbf{v}$ , and  $\mathbf{i}_o$

$$\begin{aligned} \mathbf{v}_f &= v_{f\alpha} + jv_{f\beta} = T_{3/2} [v_{fa} \ v_{fb} \ v_{fc}]^T \\ \mathbf{i}_f &= i_{f\alpha} + ji_{f\beta} = T_{3/2} [i_{fa} \ i_{fb} \ i_{fc}]^T \\ \mathbf{v} &= v_{\alpha} + jv_{\beta} = T_{3/2} [v_{an} \ v_{bn} \ v_{cn}]^T \\ \mathbf{i}_o &= i_{o\alpha} + ji_{o\beta} = T_{3/2} [i_{oa} \ i_{ob} \ i_{oc}]^T \end{aligned} \quad (5)$$

with the Clarke transformation as

$$T_{3/2} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}. \quad (6)$$

The dynamic model of a second-order  $LC$  filter in  $s$  domain is depicted in Fig. 3. Correspondingly, the continuous-time dynamic model is derived as

$$\frac{d\mathbf{v}_f}{dt} = \frac{1}{C_f} (\mathbf{i}_f - \mathbf{i}_o) \quad (7)$$

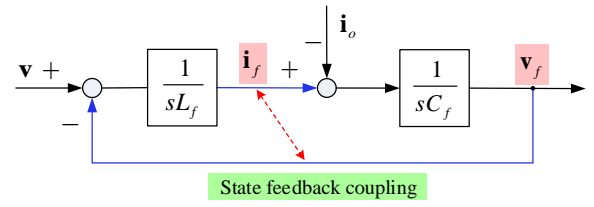


Fig. 3. Dynamic model of a second-order  $LC$  filter in  $s$  domain.

$$\frac{d\mathbf{i}_f}{dt} = \frac{1}{L_f} (\mathbf{v} - \mathbf{v}_f) \quad (8)$$

where  $L_f$  and  $C_f$  are filter inductance and capacitance.  $\mathbf{v}_f$  and  $\mathbf{i}_f$  are directly measured.  $\mathbf{i}_o$  can either be observed or measured, and the latter is employed in this paper [23].

### C. State-Feedback Coupling of $LC$ Filter

Based on the dynamics in (7), (8), and Fig. 3, it can be seen that there exists a cross-coupling effect between the system state variables: inductor current  $\mathbf{i}_f$  and capacitor voltage  $\mathbf{v}_f$ . To be specific, the voltage dynamics in (7) are related to the inductor current, while the inductor current dynamics in (8) are also influenced by the capacitor voltage. This cross-coupling effect makes it more difficult to control the capacitor voltage in  $LC$ -filtered VSIs compared to the current in  $L$ -filtered VSIs since capacitor voltage is indirectly regulated by the inductor current (which cannot be directly influenced by the controller) instead of the inverter voltage (which is directly influenced by the controller). It should be noted that system performance may be significantly degraded if this coupling effect is not properly tackled [22].

## III. CONVENTIONAL FS-MPC AND ITS LIMITATIONS

### A. Conventional Predictive Model

Based on the dynamic model in (7) and (8), the discrete predictive model of an  $LC$ -filtered VSI is formulated as

$$\underbrace{\begin{bmatrix} \mathbf{i}_{f,k+1}^p \\ \mathbf{v}_{f,k+1}^p \end{bmatrix}}_{\mathbf{x}_{k+1}} = \underbrace{\begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix}}_{\Phi} \underbrace{\begin{bmatrix} \mathbf{i}_{f,k} \\ \mathbf{v}_{f,k} \end{bmatrix}}_{\mathbf{x}_k} + \underbrace{\begin{bmatrix} \Gamma_{11} & \Gamma_{12} \\ \Gamma_{21} & \Gamma_{22} \end{bmatrix}}_{\Gamma} \underbrace{\begin{bmatrix} \mathbf{v}_k \\ \mathbf{i}_{o,k} \end{bmatrix}}_{\mathbf{u}_k} \quad (9)$$

where the coefficient matrices are calculated by

$$\begin{aligned} \Phi &= e^{\mathbf{A}T_s}, \Gamma = \int_0^{T_s} e^{\mathbf{A}\tau} \mathbf{B} d\tau, \\ \mathbf{A} &= \begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{C_f} \end{bmatrix} \end{aligned} \quad (10)$$

and  $T_s$  is the sampling period.

### B. Delay Compensation

In digital implementations, to compensate the inherent one-step computational delay, a two-step forward prediction approach is employed, which is implemented by predicting the  $(k+2)$ th instant predicted capacitor voltage  $\mathbf{v}_{f,k+2}^p$  based on the  $(k+1)$ th instant predicted values in (9) as

$$\mathbf{v}_{f,k+2}^p = \Phi_{21} \mathbf{i}_{f,k+1}^p + \Phi_{22} \mathbf{v}_{f,k+1}^p + \Gamma_{21} \mathbf{v}_{k+1} + \Gamma_{22} \mathbf{i}_{o,k+1} \quad (11)$$

where  $\mathbf{i}_{o,k+1}$  can be substituted by  $\mathbf{i}_{o,k}$  since the dynamics of load current are very slow [23].

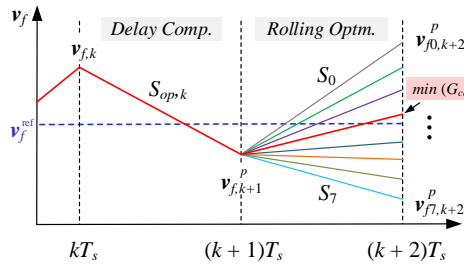


Fig. 4. Rolling-optimization principle of conventional FS-MPC.

### C. Cost Function Design and Optimal Vector Selection

Generally, the primary control objective of *LC*-filtered VSIs is to track the reference output capacitor voltage. Hence, the cost function for conventional FS-MPC schemes is designed to minimize the voltage-tracking error below [5]

$$G_{con} = \left\| \mathbf{v}_f^{\text{ref}} - \mathbf{v}_{f,k+2}^p \right\|^2 \quad (12)$$

where  $\mathbf{v}_f^{\text{ref}}$  is the reference output voltage, and  $\mathbf{v}_{f,k+2}^p$  is the compensated predicted voltage obtained from (11).

Next, to select the optimal voltage vector or switching state, the rolling-optimization technique is employed to minimize the cost function. The operating principle of rolling optimization is depicted in Fig. 4. To be specific, the delay compensation is first conducted to estimate the  $(k+1)$ th instant output voltage. Then, by enumerating all possible voltage vectors  $\mathbf{v}_{k+1}$  in (11), the one that can minimize the cost function (12) is finally determined as the optimal voltage vector and applied to VSIs (see the red line in Fig. 4).

### D. Variable Switching Frequency

It can be deduced from Fig. 4 that conventional FS-MPC only applies one voltage vector in a control period. To analyze its switching frequency, Fig. 5 shows two cases of the switching pulses generated by conventional FS-MPC schemes, where  $T_{sw} = 1/f_{sw}$  is the switching period. Since the optimal switching state is directly performed per  $T_s = 1/f_s$ , the resulting switching frequency is variable. Fig. 5 (a) depicts a case of 50 % pulse width, which generates a maximum switching frequency of  $f_{sw}$ , i.e., half of the sampling frequency. Either increase or decrease from 50 % pulse width will reduce the switching frequency, such as a case in Fig. 5 (b) with a 66.7 % pulse width. Hence, a sufficiently high sampling frequency is required to obtain an effective switching frequency, i.e., desired steady-state performance. It is worth mentioning that a variable switching frequency may cause the drawbacks like large steady-state error, spread harmonic spectrum, and complex output-filter design.

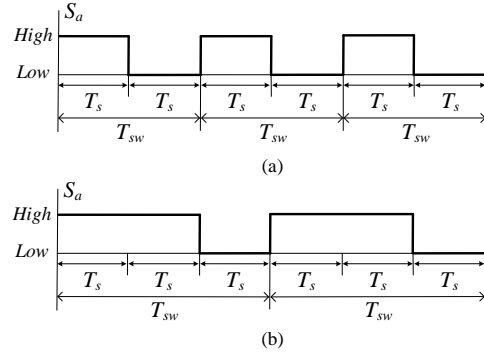


Fig. 5. Variable switching-frequency pulses analysis of conventional FS-MPC. (a) Maximum switching frequency. (b) Decreased switching frequency.

TABLE II  
CANDIDATE VECTOR SWITCHING SEQUENCE

Sector $i$	Candidate vector switching sequence $v_{si}$
1	{0 1 2 7 7 2 1 0}
2	{0 3 2 7 7 2 3 0}
3	{0 3 4 7 7 4 3 0}
4	{0 5 4 7 7 4 5 0}
5	{0 5 6 7 7 6 5 0}
6	{0 1 6 7 7 6 1 0}

construction, vector duration calculation, cost function minimization and OSS selection, duty ratio calculation, and pulse generation. The design procedures are elaborated below.

### A. Improved Vector Switching Sequence

Prior OSS-MPC scheme employs a 12-sector-6-segment vector switching sequence [20]. To reduce the computational burden and the steady-state output ripple and THD, considering the switching-transition minimization, an improved 6-sector-8-segment vector switching sequence is proposed in this paper, which is depicted in Table II. Since the sector number of the proposed vector switching sequence is decreased, the computational burden is somewhat decreased.

In essence, the proposed candidate vector switching sequence aims to resemble the switching pattern of a saddle-backed space vector modulation, which can inherently achieve an excellent steady-state performance and a fixed switching frequency [24]. To be specific, for each sector in Fig. 2, two adjacent active voltage vectors and one zero voltage vector are symmetrically applied to the 8 segments in a  $T_s$  (i.e., last 4 segments are equivalent to the first ones, but they occur in a reversed order). Consequently, the proposed space-vector-modulation-like vector switching sequence in  $i$ th sector can be described as

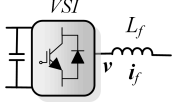
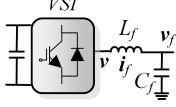
$$\mathbf{v}_{si} = \{\mathbf{v}_{v_{si}(0)}, \mathbf{v}_{v_{si}(1)}, \dots, \mathbf{v}_{v_{si}(7)}\} \quad (13)$$

where the subscript  $v_{si} = \{v_{si}(0), v_{si}(1), \dots, v_{si}(7)\}$  is listed in Table II.

It is worth mentioning that the proposed vector switching sequence performs more voltage-vector actions per  $T_s$



TABLE III  
GRADIENT-CALCULATION COMPARISON OF  $L$  AND  $LC$ -FILTERED VSIS

Comparative Item	$L$ -filtered VSI	$LC$ -filtered VSI
VSI Topology		
System order	First-order	Second-order
Dynamic model	$L_f \frac{di_f}{dt} = \mathbf{v}$	(7), (8)
State cross-coupling	No	Yes
Control objective	Inductor current	Capacitor voltage
Gradient calculation	$\frac{di_f}{dt} = \frac{1}{L_f} \mathbf{v}$	$\frac{dv_f}{dt} = \frac{1}{C_f} (\mathbf{i}_f - \mathbf{i}_o)$ (7)

compared to prior vector switching sequence in [20], thus improved steady-state performance can be achieved. After defining the candidate vector switching sequence for each sector, it is crucial to build the trajectory-based predictive voltage model, i.e., the capacitor-voltage gradient and duration candidate using vector switching sequence in Table II.

### B. Capacitor-Voltage Gradient Calculation

1) *Calculation Challenge of Voltage Gradient:* Comparison of topology, system order and dynamic model between  $L$ -filtered VSIs and  $LC$ -filtered VSIs are illustrated in Table III. As is shown, for the first-order  $L$ -filtered VSIs, the changing rate of  $\mathbf{i}_f$  is directly related to VSI's voltage vector  $\mathbf{v}$ . Hence, the gradient of  $\mathbf{i}_f$  for each voltage vector in (13) can be easily obtained using the current dynamic model (8). Similarly, for the second-order  $LC$ -filtered VSIs, the gradient of the capacitor voltage  $\mathbf{v}_f$  is calculated by (7) as

$$\begin{cases} f_{v_{\alpha},k} = \frac{dv_{f\alpha}}{dt} = \frac{1}{C_f} (i_{f\alpha,k} - i_{o\alpha,k}) \\ f_{v_{\beta},k} = \frac{dv_{f\beta}}{dt} = \frac{1}{C_f} (i_{f\beta,k} - i_{o\beta,k}) \end{cases} \quad (14)$$

where  $f_{v_{\alpha},k}$  and  $f_{v_{\beta},k}$  are capacitor-voltage gradients.

Notably, the voltage gradients in (14) are not directly related to the vector switching sequence in Table II. This is due to the state cross-coupling of the  $LC$  filter, i.e., the output capacitor-voltage gradient is regulated by the inductor current instead of the inverter voltage vector. As a result, it is not possible to directly predict the future capacitor voltage gradients for each voltage vector, and the OSS cannot be directly implemented for  $LC$ -filtered VSIs and higher-order systems.

2) *Proposed Generalized Solution:* To solve this problem, a 'one-step estimation' strategy is proposed. Note from (7) and (8) that the inductor current can indirectly build the relationship between candidate vector switching sequence and capacitor voltage gradient. Hence, based on (8), the one-step estimation of the inductor current generated by each vector switching sequence is derived using Euler discretization as

$$\begin{cases} \hat{i}_{f\alpha n,k} |_{n \in \{0,1,2\}} = i_{f\alpha,k} + \frac{T_s}{L_f} (v_{v_{si}(n)\alpha,k} - v_{f\alpha,k}) \\ \hat{i}_{f\beta n,k} |_{n \in \{0,1,2\}} = i_{f\beta,k} + \frac{T_s}{L_f} (v_{v_{si}(n)\beta,k} - v_{f\beta,k}) \end{cases} \quad (15)$$

where  $\hat{i}_{f\alpha n,k}$  and  $\hat{i}_{f\beta n,k}$  are  $k$ th instant estimated inductor currents when applying each of a zero vector ( $n = 0$ ) and two different active vectors ( $n = 1, 2$ ) of the vector switching sequence in Table II.

Then, substituting the  $k$ th instant estimated inductor current in (15) into the measured one in (14), the capacitor-voltage gradient is obtained by

$$\begin{cases} f_{v_{\alpha n},k} |_{n \in \{0,1,2\}} = \frac{1}{C_f} (\hat{i}_{f\alpha n,k} - i_{o\alpha,k}) \\ f_{v_{\beta n},k} |_{n \in \{0,1,2\}} = \frac{1}{C_f} (\hat{i}_{f\beta n,k} - i_{o\beta,k}). \end{cases} \quad (16)$$

It is important to mention that the proposed solution can simply tackle the state cross-coupling effect of an  $LC$  filter and provides a generalized way to calculate the control-variable gradients for high-order systems. Hence, it is possible to extend the OSS to higher-order systems, such as  $LCL$ -filtered VSIs, which will be verified in Section IV-H later.

### C. Trajectory-based Predictive Model

Combined with the vector switching sequence in Table II and the capacitor voltage gradient in (16), the predictive capacitor-voltage trajectories during one  $T_s$  is graphically depicted in Fig. 6.

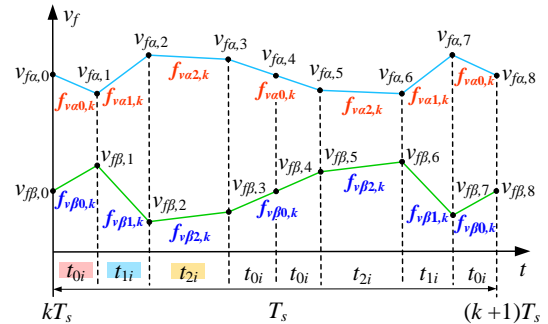


Fig. 6. Graphical depiction of predictive capacitor-voltage trajectory using a symmetrical 8-segment vector switching sequence.

According to Fig. 6, a trajectory-based capacitor voltage predictive model is constructed based on multiple capacitor-voltage gradients and vector duration  $T_i = \{t_{0i}, t_{1i}, t_{2i}\}$  as

$$\begin{cases} v_{f\alpha,k+1}^p = v_{f\alpha,k} + 2(f_{v_{\alpha 1},k}t_{1i} + f_{v_{\alpha 2},k}t_{2i} + 2f_{v_{\alpha 0},k}t_{0i}) \\ v_{f\beta,k+1}^p = v_{f\beta,k} + 2(f_{v_{\beta 1},k}t_{1i} + f_{v_{\beta 2},k}t_{2i} + 2f_{v_{\beta 0},k}t_{0i}) \end{cases} \quad (17)$$

with vector duration satisfying the following relationship

$$t_{1i} + t_{2i} + 2t_{0i} = T_s/2. \quad (18)$$

### D. Vector Duration Determination

Next, it is required to calculate the voltage-vector duration  $t_{0i}$ ,  $t_{1i}$  and  $t_{2i}$  in (17) and (18). To optimally track the capacitor-voltage reference within one control period, the optimal vector duration of each candidate vector switching sequence is derived by minimizing the sum of squared voltage-tracking errors

$$G(t_{1i}, t_{2i}) = v_{e\alpha,k+1}^2 + v_{e\beta,k+1}^2 \quad (19)$$

$$t_{1i} = \frac{(f_{v_{\beta 2},k} - f_{v_{\beta 0},k})v_{e\alpha,k} + (f_{v_{\alpha 0},k} - f_{v_{f\alpha 2},k})v_{e\beta,k} + (f_{v_{\alpha 2},k}f_{v_{\beta 0},k} - f_{v_{\alpha 0},k}f_{v_{\beta 2},k})T_s}{2(f_{v_{\alpha 0},k}f_{v_{\beta 1},k} - f_{v_{\alpha 0},k}f_{v_{\beta 2},k} + f_{v_{\alpha 1},k}f_{v_{\beta 2},k} - f_{v_{\alpha 1},k}f_{v_{\beta 0},k} + f_{v_{\alpha 2},k}f_{v_{\beta 0},k} - f_{v_{\alpha 2},k}f_{v_{\beta 1},k})} \quad (21)$$

$$t_{2i} = \frac{(f_{v_{\beta 0},k} - f_{v_{\beta 1},k})v_{e\alpha,k} + (f_{v_{\alpha 1},k} - f_{v_{f\alpha 0},k})v_{e\beta,k} + (f_{v_{\alpha 0},k}f_{v_{\beta 1},k} - f_{v_{\alpha 1},k}f_{v_{\beta 0},k})T_s}{2(f_{v_{\alpha 0},k}f_{v_{\beta 1},k} - f_{v_{\alpha 0},k}f_{v_{\beta 2},k} + f_{v_{\alpha 1},k}f_{v_{\beta 2},k} - f_{v_{\alpha 1},k}f_{v_{\beta 0},k} + f_{v_{\alpha 2},k}f_{v_{\beta 0},k} - f_{v_{\alpha 2},k}f_{v_{\beta 1},k})} \quad (22)$$

$$t_{0i} = (T_s/2 - t_{1i} - t_{2i})/2. \quad (23)$$

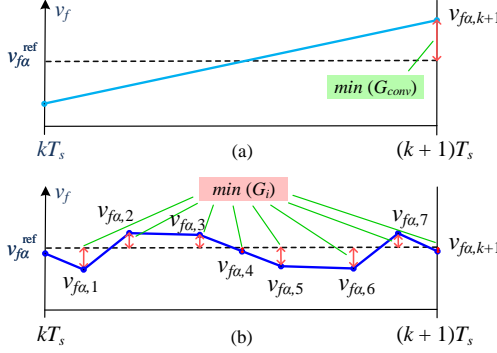


Fig. 7. Comparison of cost function minimization process ( $\alpha$  frame). (a)  $G_{con}$  in conventional FS-MPC. (b)  $G_i$  in proposed OSS-MPVC.

where  $v_{e\alpha,k+1} = v_{f\alpha}^{ref} - v_{f\alpha,k+1}^p$  and  $v_{e\beta,k+1} = v_{f\beta}^{ref} - v_{f\beta,k+1}^p$  are the predictive output voltage-tracking errors.

Then, the vector duration is obtained using the following minimal-solution conditions

$$\begin{cases} \frac{\partial G(t_{1i}, t_{2i})}{\partial t_{1i}} = 0 \\ \frac{\partial G(t_{1i}, t_{2i})}{\partial t_{2i}} = 0. \end{cases} \quad (20)$$

By solving (20), the optimal vector duration  $t_0$ ,  $t_1$  and  $t_2$  are given in (21), (22) and (23), which are shown at the top of this page (refer to Appendix A).

### E. Cost Function Minimization and OSS Selection

Since the vector duration for the vector switching sequence in Table II has been calculated, the optimal sector needs to be further selected to determine the OSS, which is obtained using FS-MPC's principle in this paper.

1) *Cost Function with Inter-Sample Behavior*: Based on the predicted capacitor voltage trajectories in Fig. 6, considering inter-sample voltage behavior at each segment during one  $T_s$ , a new cost function is formulated based on the inter-sample capacitor voltage prediction errors of each segment

$$G_i = \sum_{j=0}^7 \left( (v_{f\alpha}^{ref} - v_{f\alpha,j+1})^2 + (v_{f\beta}^{ref} - v_{f\beta,j+1})^2 \right) \quad (24)$$

with the recursive form of the predictive output capacitor voltage in each segment as

$$\begin{cases} v_{f\alpha,j+1} = v_{f\alpha,j} + f_{v_{\alpha j},k}t_{ji} \\ v_{f\beta,j+1} = v_{f\beta,j} + f_{v_{\beta j},k}t_{ji} \end{cases} \quad (25)$$

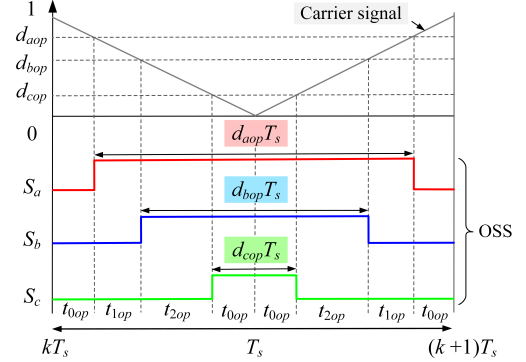


Fig. 8. Optimal duty ratio calculation based on OSS (Sector 1).

where the initial capacitor voltage  $v_{f\alpha,0} = v_{f\alpha,k}$ ,  $v_{f\beta,0} = v_{f\beta,k}$ , the gradients  $f_{v_{\alpha 0},k} = f_{v_{\alpha 3},k} = f_{v_{\alpha 4},k} = f_{v_{\alpha 7},k}$ ,  $f_{v_{\alpha 1},k} = f_{v_{\alpha 6},k}$ ,  $f_{v_{\alpha 2},k} = f_{v_{\alpha 5},k}$ , and the vector duration  $t_{0i} = t_{3i} = t_{4i} = t_{7i}$ ,  $t_{1i} = t_{6i}$ ,  $t_{2i} = t_{5i}$  due to the symmetrical switching pattern in Fig. 6. The reference  $v_f^{ref}$  can be calculated using Lagrange extrapolation technique

$$v_f^{ref} = 10v_{f,k}^{ref} - 20v_{f,k-1}^{ref} + 15v_{f,k-2}^{ref} - 4v_{f,k-3}^{ref}. \quad (26)$$

Fig. 7 shows the differences between the cost function minimization process in conventional FS-MPC and proposed OSS-MPVC with inter-sample behavior. It can be seen that the proposed cost function in (24) is different from that of the conventional FS-MPC scheme in (12). Conventional cost function only aims to minimize the capacitor-voltage tracking error at each sampling instant. In sharp contrast, the proposed cost function is based on the predictive trajectories, which aim to globally minimize the sum of squared inter-sample voltage prediction errors within one  $T_s$  (see the red arrow line in Fig. 7). As a result, the voltage gradient is optimally adjusted in multiple degrees of freedom, and the future output voltage will be controlled closer to its reference, which significantly attenuates the steady-state voltage ripple magnitude.

2) *OSS Selection and Duty Ratio Generation*: Conventional FS-MPC schemes enumerates 8 single voltage vectors in one  $T_s$  for cost function minimization as shown in Fig. 4. Follow the same principle, the proposed OSS-MPVC enumerates 6 candidate vector switching sequences defined in Table II during each control period. To be specific, by enumerating each sector  $i$  in Table II for the evaluation of  $G_i$  in (24), the one that minimizes  $G_i$  becomes the optimal sector:  $i = op$ , and the corresponding vector switching sequence becomes the OSS:  $\mathbf{v}_{si} = \mathbf{v}_{sop}$  with the optimal vector duration as  $T_{op} = \{t_{0op}, t_{1op}, t_{2op}\}$ .

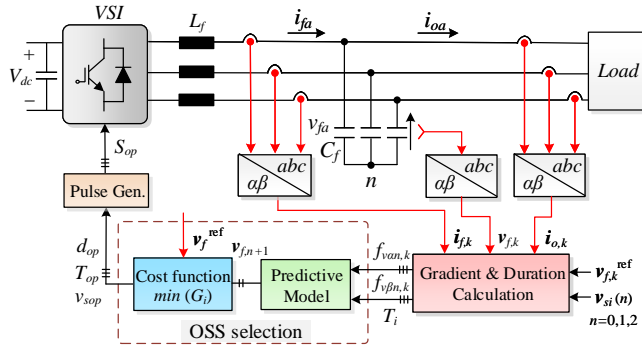


Fig. 9. Block diagram of the proposed OSS-MPVC scheme.

Further, the optimal duty ratio of the obtained OSS above is derived in view of the digital implementation. Fig. 8 shows a calculating example of the optimal duty ratio  $d_{op}$  with an optimal sector  $i = 1$  (i.e., OSS:  $\mathbf{v}_{s1}$ ). By calculating the ratio of the high-level duration to the sampling period  $T_s$  using the obtained OSS, the optimal duty ratio can be derived as

$$\begin{cases} d_{a,op} = 2(S_{a,v_{sop}(1)}t_{1op} + S_{a,v_{sop}(2)}t_{2op} + t_{0op})/T_s \\ d_{b,op} = 2(S_{b,v_{sop}(1)}t_{1op} + S_{b,v_{sop}(2)}t_{2op} + t_{0op})/T_s \\ d_{c,op} = 2(S_{c,v_{sop}(1)}t_{1op} + S_{c,v_{sop}(2)}t_{2op} + t_{0op})/T_s. \end{cases} \quad (27)$$

### F. Control-Delay and Dead-Time Compensation

1) *Control-Delay Compensation*: In digital implementations, there is an inherent computational delay, which may deteriorate the output-voltage performance [8]. To tackle this issue, a two-step ahead prediction technique should be employed [23]. Nevertheless, it is worth mentioning that unlike conventional FS-MPC schemes with only one vector action per control cycle, the proposed scheme performs multi-vector actions. Hence, conventional delay compensation strategy in (11) should be modified for proposed multi-vector OSS-MPVC. As shown in Fig. 6, the  $k$ th instant initial voltage  $v_{f\alpha,0}$  and  $v_{f\beta,0}$  in (25) should be first updated with their  $(k+1)$ th instant values using (17)

$$\begin{cases} v_{f\alpha,k+1}^p = v_{f\alpha,k} + 2(f_{v_{\alpha 1,k}}t_{1op} + f_{v_{\alpha 2,k}}t_{2op} + 2f_{v_{\alpha 0,k}}t_{0op}) \\ v_{f\beta,k+1}^p = v_{f\beta,k} + 2(f_{v_{\beta 1,k}}t_{1op} + f_{v_{\beta 2,k}}t_{2op} + 2f_{v_{\beta 0,k}}t_{0op}) \end{cases} \quad (28)$$

where  $f_{v_{\alpha n,k}}$ ,  $f_{v_{\beta n,k}}$  and  $t_{0op}$ ,  $t_{1op}$ ,  $t_{2op}$  are optimal capacitor-voltage gradients and vector duration obtained by the OSS (i.e.,  $\mathbf{v}_{v_{sop}(n),k}$ ) in the previous control period.

Second, the  $k$ th instant capacitor-voltage gradients  $f_{v_{\alpha n,k}}$  and  $f_{v_{\beta n,k}}$  in (16) should be updated with their  $(k+1)$ th instant values using one-step forward recursion

$$\begin{cases} f_{v_{\alpha n,k+1}} |_{n \in \{0,1,2\}} = \frac{1}{C_f}(\hat{i}_{f\alpha n,k+1} - i_{o\alpha,k}) \\ f_{v_{\beta n,k+1}} |_{n \in \{0,1,2\}} = \frac{1}{C_f}(\hat{i}_{f\beta n,k+1} - i_{o\beta,k}). \end{cases} \quad (29)$$

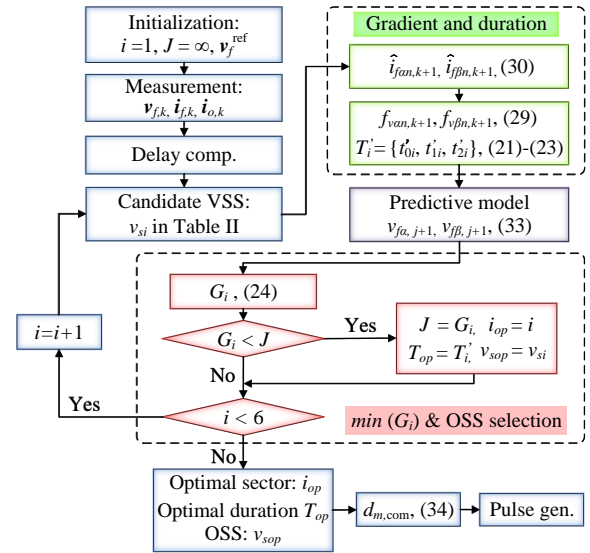


Fig. 10. Flowchart of the proposed OSS-MPVC.

In (29), the  $(k+1)$ th instant estimated inductor current  $\hat{i}_{f\alpha n,k+1}$  and  $\hat{i}_{f\beta n,k+1}$  can be derived based on (15)

$$\begin{cases} \hat{i}_{f\alpha n,k+1} = i_{f\alpha,k+1}^p + \frac{T_s}{L_f}(v_{v_{si}(n)\alpha,k+1} - v_{f\alpha,k+1}^p) \\ \hat{i}_{f\beta n,k+1} = i_{f\beta,k+1}^p + \frac{T_s}{L_f}(v_{v_{si}(n)\beta,k+1} - v_{f\beta,k+1}^p) \end{cases} \quad (30)$$

where  $v_{f\alpha,k+1}^p$  and  $v_{f\beta,k+1}^p$  have been already obtained by (28), while  $i_{f\alpha,k+1}^p$  and  $i_{f\beta,k+1}^p$  can be predicted by

$$\begin{cases} i_{f\alpha,k+1}^p = i_{f\alpha,k} + 2(f_{i_{\alpha 1,k}}t_{1op} + f_{i_{\alpha 2,k}}t_{2op} + 2f_{i_{\alpha 0,k}}t_{0op}) \\ i_{f\beta,k+1}^p = i_{f\beta,k} + 2(f_{i_{\beta 1,k}}t_{1op} + f_{i_{\beta 2,k}}t_{2op} + 2f_{i_{\beta 0,k}}t_{0op}) \end{cases} \quad (31)$$

where the  $k$ th instant inductor-current gradient is obtained by (8) using the OSS ( $\mathbf{v}_{v_{sop}(n),k}$ ) in previous control period as

$$\begin{cases} f_{i_{\alpha n,k}} |_{n \in \{0,1,2\}} = \frac{1}{L_f}(v_{v_{sop}(n)\alpha,k} - v_{f\alpha,k}) \\ f_{i_{\beta n,k}} |_{n \in \{0,1,2\}} = \frac{1}{L_f}(v_{v_{sop}(n)\beta,k} - v_{f\beta,k}). \end{cases} \quad (32)$$

Third, the vector duration  $t_{0i}$ ,  $t_{1i}$  and  $t_{2i}$  in (21), (22) and (23) should also be modified with their  $(k+1)$ th instant values  $t'_{0i}$ ,  $t'_{1i}$  and  $t'_{2i}$  based on the  $(k+1)$ th instant gradients in (29) and  $v_{e\alpha,k+1} = v_{f\alpha}^{\text{ref}} - v_{f\alpha,k+1}^p$ ,  $v_{e\beta,k+1} = v_{f\beta}^{\text{ref}} - v_{f\beta,k+1}^p$ .

In summary, compared with the uncompensated predictive voltage in (25), the predicted output voltage with control-delay compensation is expressed as

$$\begin{cases} v_{f\alpha,j+1} = v_{f\alpha,j} + f_{v_{\alpha j,k+1}}t'_{ji} \\ v_{f\beta,j+1} = v_{f\beta,j} + f_{v_{\beta j,k+1}}t'_{ji}. \end{cases} \quad (33)$$

2) *Dead-Time Compensation*: Practically, the dead time is normally inserted to avoid the breakdown of the VSIs' legs. However, the dead-time effect causes the output-voltage deviation and deteriorates the steady-state performance as well. To compensate this effect, a simple dead-time compensation strategy is adopted [25]. By online correcting the optimal duty



TABLE IV  
COMPARISON BETWEEN PROPOSED OSS-MPVC AND PRIOR MPC SCHEMES

Item description	Conventional FS-MPC [5]	Deadbeat MPC [14]	Prior OSS-MPC [20]	Proposed OSS-MPVC
Predictive model	Based on dynamics	Based on dynamics	Based on trajectory	Based on trajectory
Cost function	$G_{con} = \ \mathbf{v}_f^{\text{ref}} - \mathbf{v}_{f,k+2}^p\ ^2$	$G_{con} = \ \mathbf{v}_f^{\text{ref}} - \mathbf{v}_{f,k+2}^p\ ^2$	$G_i = \sum_{i=1}^6 \ \mathbf{S}^{\text{ref}} - \mathbf{S}_i\ ^2$	$G_i = \sum_{j=0}^7 \ \mathbf{v}_f^{\text{ref}} - \mathbf{v}_{f,j+1}\ ^2$
Applicability	$L/LC$ -filtered VSI	$L/LC$ -filtered VSI	Solely for $L$ -filtered VSI	$L/LC/LCL$ -filtered VSI
Number of sector	6	6	12	6
Number of applied vector	Single vector	Multiple vectors	Multiple vectors	Multiple vectors
Segments in one $T_s$	1	8	6	8
Switching frequency	Variable	Constant	Constant	Constant
Inter-sample consideration	No	No	Yes	Yes
Multi-objective optim.	Supported	Not supported	Supported	Supported
Steady-state performance	Moderate	Good	Good	Better

ratio in (27) according to the polarity of the phase inductor current, the compensated optimal duty ratio is expressed as

$$d_{m,\text{com}}|_{m \in \{a,b,c\}} = d_{m,\text{op}} + \frac{T_d}{T_{sw}} \text{sign}(i_{fm}) \quad (34)$$

where  $T_d$  is the dead time,  $T_{sw}$  is the switching period, and  $i_{fm}$  is the phase inductor current.

The block diagram and overall flowchart of the proposed OSS-MPVC scheme are depicted in Fig. 9 and Fig. 10.

#### G. Comparison With Prior MPC Schemes

The proposed OSS-MPVC scheme is compared to prior MPC schemes in Table IV. Essentially, deadbeat MPC and OSS-based MPC methods are multi-vector MPC schemes, which can achieve reduced switching ripple and fixed switching frequency compared to single-vector FS-MPC schemes. On the one hand, conventional FS-MPC and deadbeat MPC schemes construct the predictive model based on system dynamics, while that of OSS-based MPC methods is based on the predictive trajectory. Moreover, conventional FS-MPC and deadbeat MPC schemes only consider the system behavior at each discrete sampling instant since they employ the dynamics-based predictive model. In contrast, OSS-based MPC methods fully consider inter-sample behavior due to the trajectory-based predictive model, which can further improve the steady-state performance.

On the other hand, the proposed OSS-MPVC is also different from prior OSS-MPC. First, prior OSS-MPC is solely designed for first-order  $L$ -filtered VSIs, which cannot handle the gradient-calculation issues in high-order systems, such as  $LC$  and  $LCL$ -filtered VSIs. In contrast, the proposed OSS-MPVC provides a generalized solution to extend the OSS to high-order systems. Second, the proposed 6-sector-8-segment vector switching sequence in Table II is different from that of prior OSS-MPC (12-sector-6-segment, see Table I in [20]). The proposed vector switching sequence performs more vector actions per control period and generates a saddle-backed space-vector-modulation-like duty ratio compared to prior OSS-MPC, thus achieving a lower output ripple and

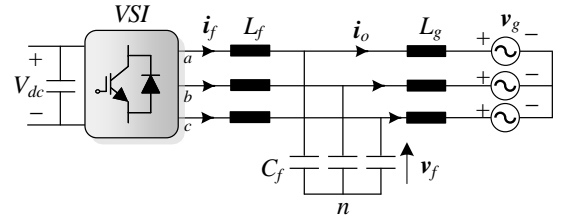


Fig. 11. Topology of an  $LCL$ -filtered grid-tied converter.

THD. To sum up, the proposed OSS-MPVC scheme can obtain the optimal steady-state output voltage with a constant switching frequency among the four MPC methods.

#### H. Extension to $LCL$ -Filtered Grid-Tied Converters

The typical topology of a third-order  $LCL$ -filtered grid-tied converter is depicted in Fig. 11. Compared to  $LC$ -filtered VSIs, the output of  $LCL$ -filtered VSIs is connected to grid instead of loads, whose primary control objective is the grid current instead of the capacitor voltage. Hence, apart from the capacitor-voltage and inductor-current dynamics in (7) and (8), additional grid-current dynamics are described as

$$\frac{d\mathbf{i}_o}{dt} = \frac{1}{L_g}(\mathbf{v}_f - \mathbf{v}_g) \quad (35)$$

where  $\mathbf{i}_o$  becomes the grid current,  $L_g$  is the equivalent grid-side inductance and  $\mathbf{v}_g$  is the grid voltage.

The design procedures of the proposed method for  $LCL$ -filtered VSIs are given to verify its versatility to third-order systems. First, the proposed vector switching sequence in Table II is retained. Then, the grid-current gradient is required, which can be derived based on the proposed generalized solution in Section IV-B as

$$\begin{cases} f_{g\alpha n,k} |_{n \in \{0,1,2\}} = \frac{1}{L_g}(\hat{v}_{f\alpha n,k} - v_{g\alpha,k}) \\ f_{g\beta n,k} |_{n \in \{0,1,2\}} = \frac{1}{L_g}(\hat{v}_{f\beta n,k} - v_{g\beta,k}) \end{cases} \quad (36)$$

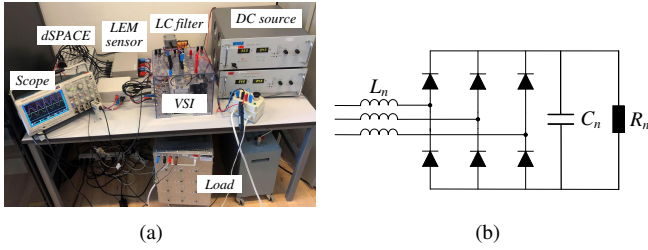


Fig. 12. Experimental configuration. (a) Testbed. (b) Nonlinear load.

TABLE V  
NOMINAL PARAMETERS OF AN LC-FILTERED VSI SYSTEM

DC bus voltage	$V_{dc} = 700 \text{ V}$
Reference voltage	$V_{ref} = 300 \text{ V}, f_{ref} = 50 \text{ Hz}$
VSI dead time	$T_d = 4 \mu\text{s}$
Output LC filter	$L_f = 2.4 \text{ mH}, C_f = 15 \mu\text{F} (f_c = 840 \text{ Hz})$
Linear load	$R_l = 60 \Omega$
Nonlinear load	$C_n = 2.2 \text{ mF}, L_n = 1.8 \text{ mH}, R_n = 460 \Omega$

where  $\hat{v}_{f\alpha n,k}$  and  $\hat{v}_{f\beta n,k}$  are the estimated capacitor voltage obtained by a one-step capacitor-voltage estimation using the voltage dynamic model in (7)

$$\begin{cases} \hat{v}_{f\alpha n,k} |_{n \in \{0,1,2\}} = v_{f\alpha,k} + \frac{T_s}{C_f} (\hat{i}_{f\alpha n,k} - i_{o\alpha,k}) \\ \hat{v}_{f\beta n,k} |_{n \in \{0,1,2\}} = v_{f\beta,k} + \frac{T_s}{C_f} (\hat{i}_{f\beta n,k} - i_{o\beta,k}) \end{cases} \quad (37)$$

where  $\hat{i}_{f\alpha n,k}$ ,  $\hat{i}_{f\beta n,k}$  are estimated inductor current in (15).

Further, the capacitor voltage  $v_{f\alpha}$ ,  $v_{f\beta}$  and its gradients  $\dot{v}_{f\alpha n,k}$ ,  $\dot{v}_{f\beta n,k}$  from (17) to (26) should be replaced by the grid current  $i_o$  and its gradients in (36).

## V. SIMULATION AND EXPERIMENTAL RESULTS

### A. Testbed Description

In order to verify the effectiveness of the proposed OSS-MPVC, comparative simulations in MATLAB/Simulink with PLECS and experiments using conventional FS-MPC in [5], deadbeat MPC in [14], and prior OSS-MPC (i.e., using prior vector switching sequence in [20]) are carried out. It should be mentioned that the same dead-time compensation strategy is deployed for all four methods to avoid its influence on performance verification. For deadbeat MPC, prior OSS-MPC, and proposed OSS-MPVC, the dead-time compensation (34) is applied. Similarly, for conventional FS-MPC, a modification of (34) is employed (i.e., replacing the duty cycle with the inverter voltage vector). Fig. 12 depicts the experimental setup, which consists of DC sources, a Semikron three-phase VSI with an output LC filter, linear resistance loads, and nonlinear loads. All the four MPC algorithms are implemented in a dSPACE DS1202 PowerPC DualCore 2-GHz processor board with the nominal parameters tabulated in Table V [23], [26]. Regarding the LC filter selection, a larger LC filter can generate a lower THD with smaller output ripples. By following [27],  $L_f = 2.4 \text{ mH}$  is selected according to the maximum allowable current ripple and  $C_f = 15 \mu\text{F}$  is chosen

TABLE VI  
COMPARISON OF SWITCHING FREQUENCY AND COMPUTATIONAL BURDEN OF FOUR MPC METHODS

Items	Sampling $f_s$	Switching $f_{asw}$	Turnaround time
Conventional FS-MPC	50 kHz	$\approx 9.6 \text{ kHz}$	13 $\mu\text{s}$
Deadbeat MPC	20 kHz	10 kHz	13 $\mu\text{s}$
Prior OSS-MPC	20 kHz	10 kHz	15 $\mu\text{s}$
Proposed OSS-MPVC	20 kHz	10 kHz	14 $\mu\text{s}$

based on the cut-off frequency and the reactive power limit (about 5% of rated power). Then, a cut-off frequency of  $f_c = 840 \text{ Hz}$  is obtained.

### B. Switching Frequency and Computational Burden

Switching frequency and computational burden of the four MPC methods are compared in Table VI. It can be deduced that the sampling frequency of deadbeat MPC, prior OSS-MPC and proposed OSS-MPVC schemes are set as 20 kHz since they produce a fixed switching frequency. However, conventional FS-MPC scheme generates a variable switching frequency, its average switching frequency  $f_{asw}$  is evaluated using the following equations [8], [28]

$$f_{asw} = \frac{\sum_{i=1}^N sw(i)}{3 \cdot N \cdot T_s} \quad (38)$$

$$sw(i) = \sum_{m=a,b,c} |S_{m,k+1} - S_{m,k}| \quad (39)$$

where  $N$  is the number of time intervals for average switching frequency calculation.  $S_{m,k+1}$  and  $S_{m,k}$  are the candidate switching state and the applied switching state in the previous step of each phase.

For a fair comparison, the sampling frequency of conventional FS-MPC is set as 50 kHz to obtain an average switching frequency of  $f_{asw} \approx 9.6 \text{ kHz}$ , which is similar to that of other three fixed-switching frequency MPC methods, 10 kHz [28]. Besides, the computational cost of the four MPC methods is compared. The total turnaround time is calculated using the dSPACE profiler, which includes A/D conversion and algorithm execution time. Since the sampling rate of the A/D converter is 1MSPS (around 1  $\mu\text{s}$ ) in dSPACE, the total turnaround time is mainly spent on the A/D conversion, around 8  $\mu\text{s}$  (including three-phase voltages, two-phase inductor currents, two-phase load current, and a DC-bus voltage). The remaining is the execution time of the MPC algorithms. It can be deduced from Table VI that the computational burden using proposed OSS-MPVC is somewhat increased (about 1  $\mu\text{s}$ ) compared to conventional FS-MPC and deadbeat MPC schemes. Nevertheless, the proposed OSS-MPVC scheme somewhat decreases the computational burden compared to prior OSS-MPC schemes.

### C. Simulation Results

Fig. 13 shows the simulation results of four MPC methods with a linear load. It can be observed that for conventional FS-MPC, the duty ratio only jumps between 0 and 1 due to the

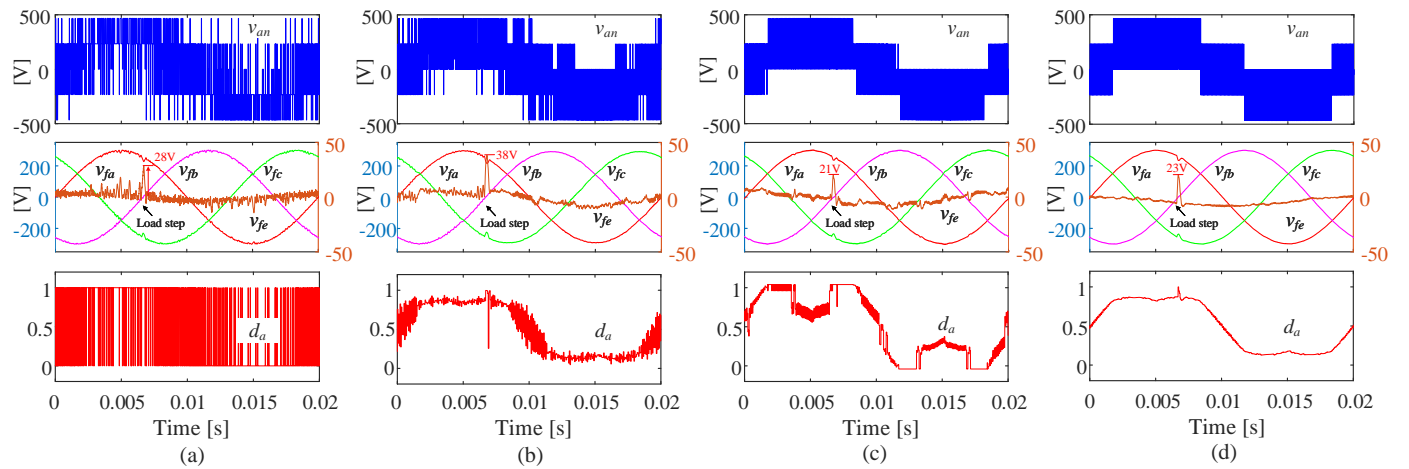


Fig. 13. Simulation comparison of four MPC methods with a linear load. [From top to bottom are phase 'a' inverter voltage, output capacitor voltage and tracking error, and duty ratio.] (a) Conventional FS-MPC. (b) Deadbeat MPC. (c) Prior OSS-MPC. (d) Proposed OSS-MPVC.

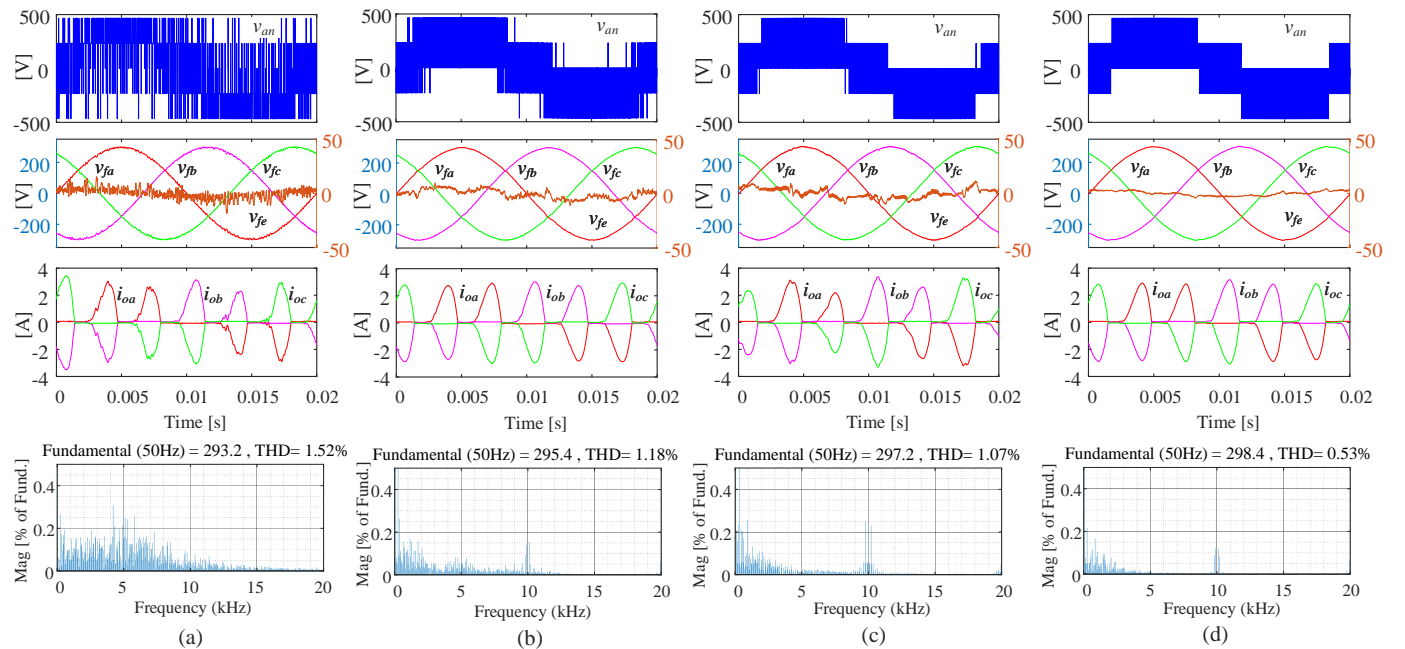


Fig. 14. Simulation comparison of four MPC methods with a nonlinear load. [From top to bottom are phase 'a' inverter voltage, output capacitor voltage and tracking error, load current and harmonic spectrum of  $v_{fa}$ .] (a) Conventional FS-MPC. (b) Deadbeat MPC. (c) Prior OSS-MPC. (d) Proposed OSS-MPVC.

single-voltage-vector action, leading to a large switching ripple. In contrast, the other three MPC schemes generate a continuous duty ratio varying from 0 to 1 due to the modulation nature. Moreover, the OSS-based MPC methods output a more compact inverter phase voltage with less non-adjacent inverter voltage jumps. Especially, the proposed OSS-MPVC achieves the smoothest saddle-backed duty ratio (without saturation) and the most intensive inverter voltage. Hence, the proposed OSS-MPVC obtains the best steady-state performance with the lowest voltage tracking error. Concerning the dynamic response under a load step change, the proposed method has a similar voltage transient recovery performance (i.e., load-disturbance rejection ability) as prior OSS-MPC but better than that of conventional FS-MPC and deadbeat MPC.

Fig. 14 shows the simulation results of four MPC methods with a nonlinear load. Still, the proposed method maintains the

best steady-state performance with the lowest tracking error. Besides, Fig. 14 reflects that the harmonic spectrum of conventional FCS-MPC is widespread, increasing the output-filter design complexity and THD. In contrast, the proposed method achieves a concentrated harmonic spectrum as deadbeat MPC and prior OSS-MPC schemes while it has the lowest THD.

Fig. 15 depicts the simulation results of the sensitivity to model mismatches using the four MPC methods, where the steady-state voltage THD and tracking root mean square error (RMSE) are shown [23]. The results reflect that the sensitivity to model mismatches using four MPC methods varies to a different degree. For conventional FS-MPC and deadbeat MPC, the steady-state performance is more sensitive to inductance mismatches. Either underestimation or overestimation of actual inductance in the controller would somewhat increase the output-voltage RMSE and THD. In contrast, the OSS-

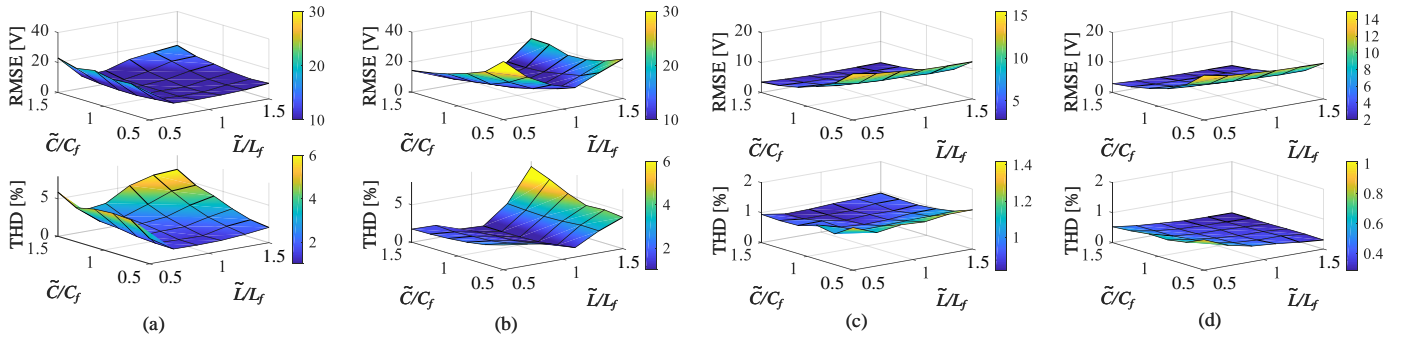


Fig. 15. Simulation comparison of four MPC methods under model mismatch of  $\tilde{L}$  and  $\tilde{C}$ . [From top to bottom are output voltage-tracking RMSE and THD of  $v_{fa}$ .] (a) Conventional FS-MPC. (b) Deadbeat MPC. (c) Prior OSS-MPC. (d) Proposed OSS-MPVC.

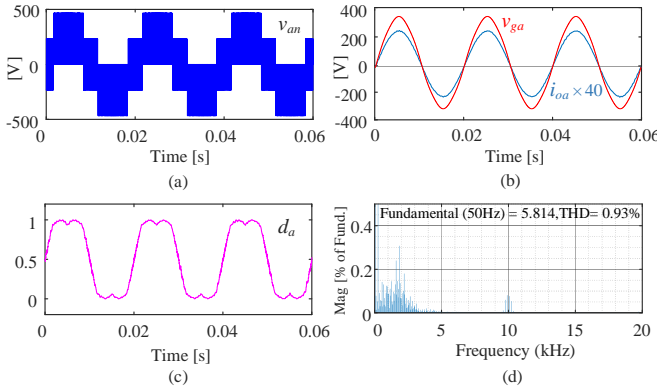


Fig. 16. Simulation results using proposed method on an  $LCL$ -filtered grid converter. (a) Inverter phase voltage. (b) Grid phase voltage and current. (c) Duty ratio. (d) Harmonic spectrum of grid current.

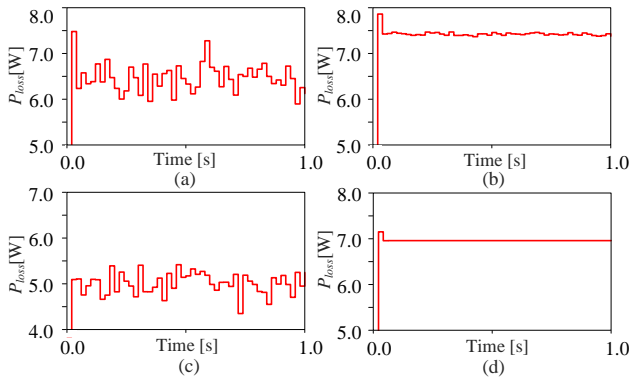


Fig. 17. Simulated average switching loss using four MPC methods with the same linear load  $R_l = 60 \Omega$ . (a) Conventional FS-MPC. (b) Deadbeat MPC. (c) Prior OSS-MPC. (d) Proposed OSS-MPVC.

based MPC methods in Figs. 15 (c) and (d) are more stable and less sensitive to model mismatches. Especially, the proposed OSS-MPVC offers the strongest robustness with the lowest RMSE and THD under various model-mismatch conditions.

Fig. 16 depicts the simulation results of the proposed method for  $LCL$ -filtered grid-tied converters to primarily verify the universality to high-order systems, where the grid-current reference  $i_o^{\text{ref}} = 6$  A, nominal grid-voltage magnitude  $V_g = 326$  V (with 5th, 7th and 11th-order harmonics), and the equivalent grid-side inductance  $L_g \approx 4$  mH. As it is shown,

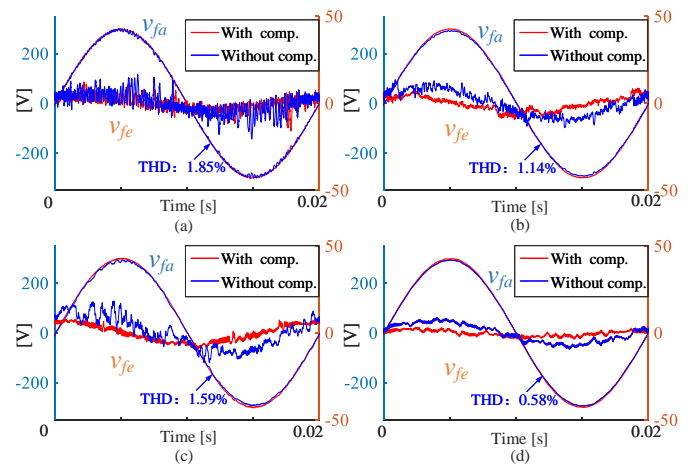


Fig. 18. Simulation results of dead-time ( $4\mu\text{s}$ ) impact on four MPC methods with and without dead-time compensation. (a) Conventional FS-MPC. (b) Deadbeat MPC. (c) Prior OSS-MPC. (d) Proposed OSS-MPVC.

the grid current is in phase with the grid voltage. As expected, the duty ratio is similar to the saddle-backed waveform as the  $LC$ -filtered VSI case in Fig. 13 (d). Moreover, the harmonic spectrum of the grid current behaves a fixed switching frequency of 10 kHz and also conforms well with the IEEE Std 1547. The results verify the applicability of the proposed method in high-order power converter systems.

To compare the switching loss with four MPC methods, the switching loss of a semiconductor in a VSI can be calculated as  $P_{\text{loss}} = f_{\text{asw}}(E_{\text{on}} + E_{\text{off}})$  with  $E_{\text{on}}$  and  $E_{\text{off}}$  as the turn-on and turn-off energy losses. It can be seen that the switching loss is affected by switching energy (a function of conducting current), switching frequency and patterns. Fig. 17 shows the simulated quantitative switching-loss comparison using four MPC methods based on PLECS with the parameters obtained from the datasheet of IGBT modules SKM 50GB123D (1200V and 40 A ratings). As it is shown, the average switching loss using FS-MPC is about 6.6 W, which is slightly lower than deadbeat MPC (about 7.4 W) and proposed OSS-MPVC (about 6.9 W) since the average switching frequency of FS-MPC is slightly lower than 10 kHz. However, the variable switching frequency of FS-MPC results in an uneven switching loss. The prior OSS-MPC generates the minimum switching loss of about 5 W since it has a



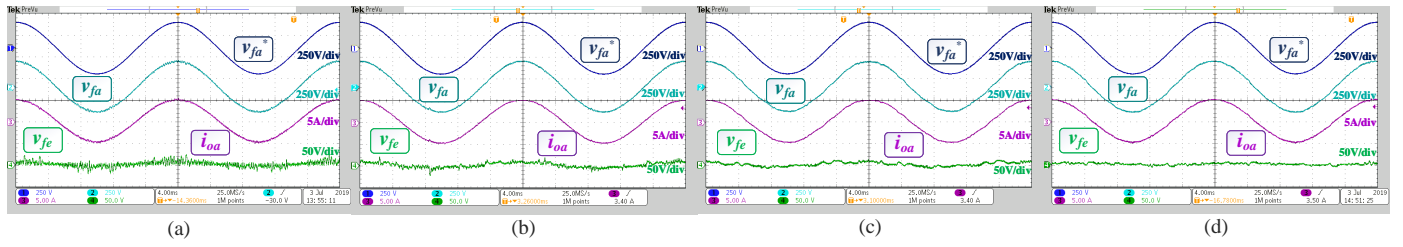


Fig. 19. Steady-state performance with a nominal linear load. (a) Conventional FS-MPC ( $v_{fe, RMSE} = 6.936$  V, THD of  $v_{fa} = 2.89\%$ ). (b) Deadbeat MPC ( $v_{fe, RMSE} = 5.695$  V, THD of  $v_{fa} = 2.32\%$ ). (c) Prior OSS-MPC ( $v_{fe, RMSE} = 4.697$  V, THD of  $v_{fa} = 2.06\%$ ). (d) Proposed OSS-MPVC ( $v_{fe, RMSE} = 2.654$  V, THD of  $v_{fa} = 1.75\%$ ).

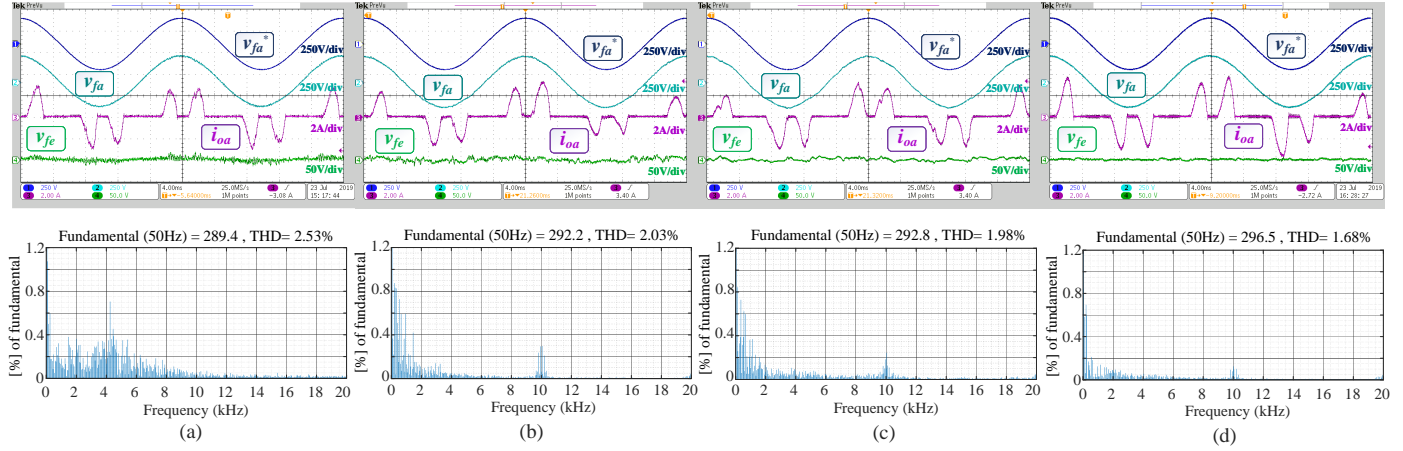


Fig. 20. Steady-state performance with a diode-rectifier-bridge nonlinear load. (a) Conventional FS-MPC ( $v_{fe, RMSE} = 4.759$  V, THD of  $v_{fa} = 2.53\%$ ). (b) Deadbeat MPC ( $v_{fe, RMSE} = 4.465$  V, THD of  $v_{fa} = 2.03\%$ ). (c) Prior OSS-MPC ( $v_{fe, RMSE} = 3.347$  V, THD of  $v_{fa} = 1.98\%$ ). (d) Proposed OSS-MPVC ( $v_{fe, RMSE} = 2.137$  V, THD of  $v_{fa} = 1.68\%$ ).

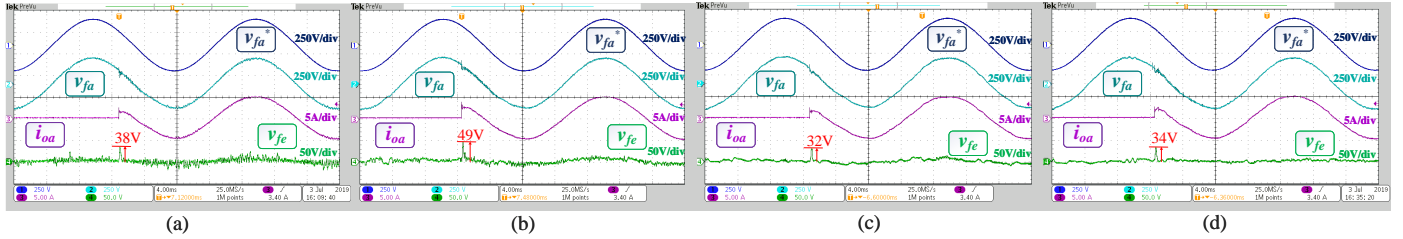


Fig. 21. Dynamic performance with a linear-load step change. (a) Conventional FS-MPC. (b) Deadbeat MPC. (c) Prior OSS-MPC. (d) Proposed OSS-MPVC.

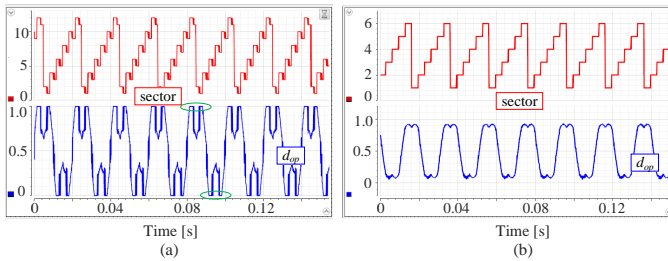


Fig. 22. Comparison of optimal sector selection and optimal duty ratio using prior and proposed vector switching sequence. [Obtained from dSPACE ControlDesk]. (a) Prior OSS-MPC. (b) Proposed OSS-MPVC.

less switch-transition number per control period (decreased by one-third) compared to deadbeat MPC and the proposed method. Nevertheless, the reduction of the switch transition somewhat increases the output ripple and harmonics. It should be mentioned that the proposed OSS-MPVC has the most

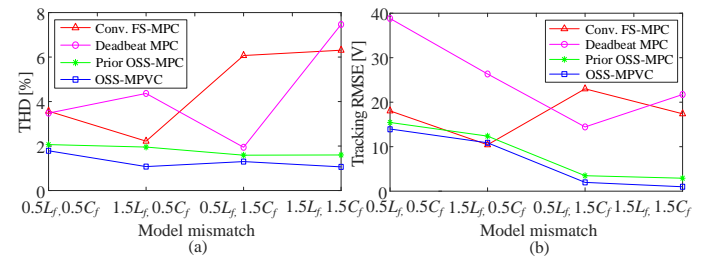


Fig. 23. Experimental results of sensitivity to model mismatches using four MPC methods. (a) THD. (b) Voltage tracking RMSE.

uniform switching-loss distribution. Considering the foremost control objective is to achieve a high-quality output voltage, the proposed method can optimally realize it with a slight sacrifice of the switching loss.

Fig. 18 evaluates the impact of dead time on the control performance using four MPC methods. It is known that a larger



dead time would result in a larger output-voltage tracking error [25]. By comparing the figures in Fig. 18, it can be deduced that the dead time causes the voltage deviations for all MPC methods (without dead-time compensation) to a varying degree. The FS-MPC and prior OSS-MPC are more sensitive to the dead-time effect, inducing larger voltage harmonics. In contrast, the proposed method is least affected by the dead time effect, generating the lowest THD similar to the case with dead-time compensation. All in all, the steady-state performance of four MPC methods can be significantly improved by employing the dead-time compensation, and the comparison of four MPC methods is fair since the same dead-time compensation strategies are deployed.

#### D. Experimental Results

1) *Steady-State Performance Comparison*: Fig. 19 and Fig. 20 show the experimental results of the steady-state response using four MPC methods under a linear load and a nonlinear load, where  $v_{fa}^*$ ,  $v_{fa}$ ,  $i_{oa}$  and  $v_{fe}$  are phase voltage reference, output voltage, load current and output voltage tracking error. The same conclusions as in simulations can be drawn that the proposed OSS-MPVC has the smallest steady-state voltage ripple magnitude and tracking RMSE among four MPC methods both under linear and nonlinear loads. Moreover, the harmonic spectra of the output voltage are shown in Fig. 20, which are plotted by MATLAB/Simulink with the experimental data obtained from the oscilloscope. It shows that conventional FS-MPC has a widespread harmonic spectrum due to the single switching action per control period, while the other three MPC methods have a concentrated harmonic spectrum and thus achieve a fixed switching frequency. In particular, the proposed OSS-MPVC results in the lowest THD and the optimal steady-state performance among four MPC methods.

2) *Dynamic Performance Comparison*: Experimental results of the dynamic response using four MPC methods with a linear load step change are depicted in Fig. 21. As expected, the experimental results are consistent with the simulation results shown in Fig. 13, where the transient voltage fluctuation using the proposed OSS-MPVC is 34 V, which is similar to that using prior OSS-MPC, 32 V. Nevertheless, the transient voltage fluctuation using the proposed OSS-MPVC is still smaller than conventional FS-MPC, 38 V, and deadbeat MPC, 49 V. Hence, the proposed method has faster dynamic response and a better load disturbance rejection ability compared to conventional FS-MPC and deadbeat MPC schemes.

3) *OSS Selection and Optimal Duty Ratio*: To verify the superiority of the proposed improved 6-sector-8-segment vector switching sequence compared to conventional 12-sector-6-segment vector switching sequence in prior OSS-MPC [19], [20], the optimal sector selection and the resulting optimal duty ratio are experimentally compared in Fig. 22. It can be deduced from Fig. 22 (a) that the optimal sector sequence of the prior OSS-MPC scheme is switched between 1 and 12. Its duty-ratio saturation area (see the green circle in Fig. 22 (a)) and 6-segment vector switching sequence in each control period will induce undesired switching ripple, which would bring adverse effect on the steady-state performance.

In contrast, from Fig. 22 (b), the proposed method has a reduced number of 6 switching sectors and a non-saturation saddle-backed duty ratio due to the 8-segment vector switching sequence in Table II. As a result, increased control degrees of freedom of the output voltage, improved steady-state performance, and reduced computational burden can be achieved by the proposed method.

4) *Sensitivity to Model Mismatch*: Quantitative experimental results of the sensitivity to mismatched  $\tilde{C}$  and  $\tilde{L}$  (i.e., changing  $\pm 50\%$  of nominal  $C_f$  and  $L_f$  in the four MPC controllers) are depicted in Fig. 23. As expected, it can be seen that both OSS-based MPC methods have similar behavior to model mismatches, i.e., prior OSS-MPC and the proposed method are less sensitive to model mismatches compared to conventional FS-MPC and deadbeat MPC schemes. Nonetheless, it should be noted that the proposed OSS-MPVC scheme still maintains the least sensitivity (strongest robustness) to model mismatches among four MPC methods with the lowest THD and voltage tracking RMSE.

## VI. CONCLUSION

This paper presents a multi-vector OSS-MPVC scheme for second-order  $LC$ -filtered VSIs, extending the applicable scope of OSS to high-order VSI systems. A reduced output-voltage ripple with a fixed switching frequency is achieved by introducing an improved vector switching sequence. The capacitor-voltage gradient calculation issue caused by the state coupling of  $LC$  filter is solved by proposing a ‘one-step estimation’ technique, which provides a generalized solution to implement the OSS for higher-order systems. The inter-sample voltage dynamics are considered in the cost function, further attenuating the output ripple. Generalized control delay and dead-time compensation scheme for OSS-based MPC schemes are also derived. Simulation and experimental results verify the superiority of the proposed OSS-MPVC.

### APPENDIX A

#### CALCULATION OF VECTOR DURATION

The voltage-vector duration  $T_i = \{t_{0i}, t_{1i}, t_{2i}\}$  in (21), (22) and (23) can be calculated based on (20), which yields

$$\begin{aligned}
 & \frac{\partial G(t_{1i}, t_{2i})}{\partial t_{1i}} \\
 &= 2v_{e\alpha, k+1} \frac{\partial v_{e\alpha, k+1}}{\partial t_{1i}} + 2v_{e\beta, k+1} \frac{\partial v_{e\beta, k+1}}{\partial t_{1i}} \\
 &= 2v_{e\alpha, k+1} \frac{\partial(v_{e\alpha, k} - 2f_{v\alpha 1, k}t_{1i} - 2f_{v\alpha 2, k}t_{2i} - 4f_{v\alpha 0, k}t_{0i})}{\partial t_{1i}} \\
 &+ 2v_{e\beta, k+1} \frac{\partial(v_{e\beta, k} - 2f_{v\beta 1, k}t_{1i} - 2f_{v\beta 2, k}t_{2i} - 4f_{v\beta 0, k}t_{0i})}{\partial t_{1i}} \\
 &= 4v_{e\alpha, k+1}(f_{v\alpha 0, k} - f_{v\alpha 1, k}) + 4v_{e\beta, k+1}(f_{v\beta 0, k} - f_{v\beta 1, k}) \\
 &= 4 \left( v_{e\alpha, k} + 2(f_{v\alpha 0, k} - f_{v\alpha 1, k})t_{1i} \right. \\
 &\quad \left. + 2(f_{v\alpha 0, k} - f_{v\alpha 2, k})t_{2i} - f_{v\alpha 0, k}T_s \right) (f_{v\alpha 0, k} - f_{v\alpha 1, k}) \\
 &+ 4 \left( v_{e\beta, k} + 2(f_{v\beta 0, k} - f_{v\beta 1, k})t_{1i} \right. \\
 &\quad \left. + 2(f_{v\beta 0, k} - f_{v\beta 2, k})t_{2i} - f_{v\beta 0, k}T_s \right) (f_{v\beta 0, k} - f_{v\beta 1, k}) \\
 &= 0.
 \end{aligned} \tag{40}$$

Similar treatment can be done for  $\frac{\partial G(t_{1i}, t_{2i})}{\partial t_{2i}} = 0$ . Then, by offline solving the resulting equation set,  $t_{1i}$ ,  $t_{2i}$  and  $t_{0i}$  can be obtained, which are shown in (21), (22) and (23).

#### ACKNOWLEDGMENT

J. Rodriguez acknowledges the support of ANID through projects FB0008, ACT192013 and 1170167.

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